Yet another alternative involves a departure at the stages of FIG. 4 and FIGS. 13C or 18, with the result shown in FIG. 21. Instead of depositing a contiguous polysilicon layer 32 (FIG. 4), two successive polysilicon layers 32A, 32B, each of a thickness, e.g., of about 1 μm., are deposited, with an intervening oxidation step. In the etching step (FIGS. 13C or 18) to form trench 63, the oxide layer 90 (e.g., 1000 angstroms) serves as an etch stop to protect the first polysilicon layer 32A. Layer 32A is N-doped to a resistivity conventionally used in polysilicon contacts. Doping can be done before depositing layer 32B or after removing it, such as the step shown in FIG. 14A. Layer 32A can serve as the gate conductive layer without metallization, although deposition of gate metal after removal of oxide layer 90 is preferred for high speed devices.

Accordingly, one should now see how the method proposed by the invention offers a dramatic improvement over the best-known prior art procedures. Mask-dependent, catastrophic errors or defects in a finally produced semiconductor device are obviated. Doping is precisely and effectively controlled to minimize parasitics. Conductive contacts for both the source and gate can be formed in one step and effectively isolated without separate masks. As a significant consequence, the entire usable area of a silicon wafer can be employed with assurance, even in the manufacture of a single, extremely large device, that it will be free from a mask-dependent failure.

In addition to the advantages discussed above which result from employment of the method of the present invention, there are certain others which are worth noting. By minimizing the number of masking steps required, manufacturing time and the number of required manufacturing personnel are reduced. Also, less expensive processing equipment can be used than is now required. Additionally, by shrinking the overall processing time, this reduces the work-in-process inventory, and, of course, such is an important expense consideration. Employing the technique of the invention in the computer-controlled laser/ion beam applications, one can design and generate a semiconductor device easily in an extremely short period of time.

Yet another advantage offered by the invention is that it eliminates the kind of defects which can result from temperature and humidity changes that can occur in the working environment over the time required to complete multiple masking steps. The mask-surrogate pattern-definers which are created, built into the structure as they are, eliminate these possibilities.

Thus, one should see how the important objects of the invention, and the advantages claimed for it, are readily obtained The teachings of the invention are not limited to a recessed-source power MOSFET. For example, they can be applied advantageously to a recessed-gate process and structure.

Having described and illustrated the principles of our invention in a preferred embodiment and variations thereof, it should be apparent to those skilled in the art that the invention may be modified in arrangement and detail without departing from such principles. We claim all modifications coming within the scope and spirit of the following claims.

We claim:

1. A method of producing a MOS device on a semiconductor substrate upper surface, said method comprising:

forming a first oxide layer of a first thickness on the substrate upper surface,

forming a protective layer comprising a polysilicon layer of an initial thickness over the oxide layer,

patterning the protective layer in accordance with a defined outline characteristic,

exposing a portion of the upper surface of the semiconductor substrate within a boundary determined by the defined outline characteristic,

simultaneously etching silicon in the exposed substrate portion and in the protective layer to form a trench with a base and sidewalls of a first depth and to remove a portion of the initial thickness of the polysilicon layer leaving a remaining portion of the polysilicon layer on the first oxide layer, and

depositing conductive material to form a first conductive layer on the substrate in the base of the trench,

the remaining portion of the polysilicon layer being doped so as to form a second conductive layer, the first conductive layer being vertically spaced from the second conductive layer by at least the thickness of the first oxide layer so as to be electrically separated therefrom.

2. A method according to claim 1 in which the polysilicon layer of said initial thickness is formed by a first, doped polysilicon layer in contact with the first oxide layer, a second polysilicon layer atop the first polysilicon layer, and an etch-stopping layer sandwiched between the first and second polysilicon layers to limit removal to the second polysilicon layer.

3. A method according to claim 1 including forming a sidewall spacer on each side of the protective layer with a vertical dimension approximately equal to the sum of the first oxide layer thickness and the initial thickness of the protective layer.

4. A method according to claim 1 in which the conductive-material deposition step also forms a gate conductive layer atop the doped protective layer.

5. A method according to claim 4 in which the conductive material is a metal.

6. A method according to claim 4 including laterally confining the gate conductive layer to an area atop the doped protective layer.

7. A method of producing a MOS device on a semiconductor substrate upper surface, said method comprising:

forming a first oxide layer of a first thickness on the substrate upper surface,

depositing a first polysilicon layer in contact with the first oxide layer,

doping the first polysilicon layer,

forming an etch-stopping oxide layer atop the first polysilicon layer,

depositing a second polysilicon layer atop the etch-stopping oxide layer, first polysilicon layer and first oxide, the first polysilicon layer, etch-stopping oxide layer, and second polysilicon layer each having a predetermined thickness and forming a protective layer,

patterning the protective layer in accordance with a defined outline characteristic,

exposing a portion of the upper surface of the semiconductor substrate within a boundary determined by the defined outline characteristic,

selectively etching silicon in the exposed substrate portion to form a trench with a base and sidewalls of a first depth and in the protective layer to re-